IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. YAMAZAKI, et al.
Serial No.:	10/639,465
Filed:	AUGUST 13, 2003
Title:	FABRICATION METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Group AU:	1763
Examiner:	George A. Goudreau
Confirm. No.:	6745

AMENDMENT

Mail Stop: AMEND – FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

January 22, 2007

SIR:

In response to the Office Action mailed September 20, 2006, the period of response having been extended for one (1) month by the attached Petition for Extension of Time, please amend the above-identified application as listed in the following, and as set forth on the following pages:

AMENDMENTS TO THE CLAIMS; and

REMARKS are included following the amendments.